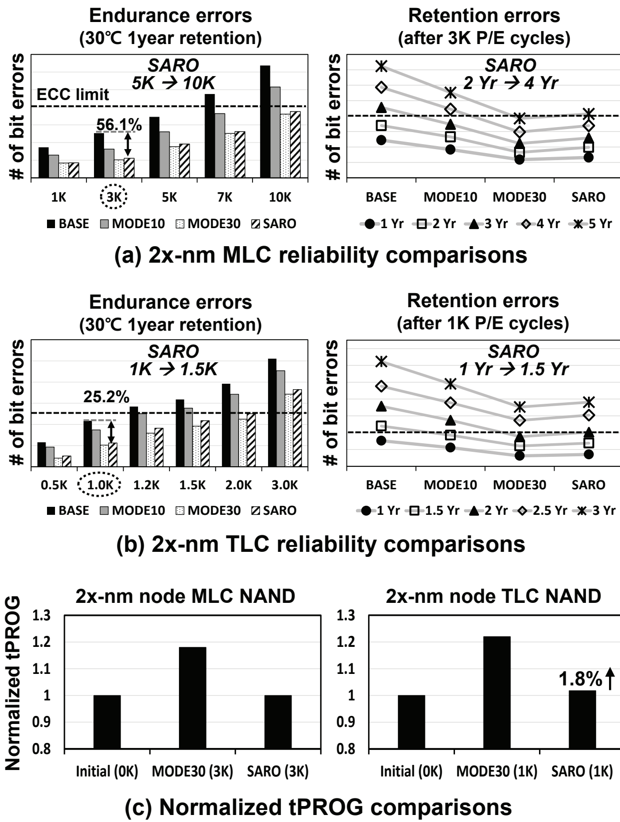

Figure 11: Comparisons of reliability and performance metrics of four different operation modes.

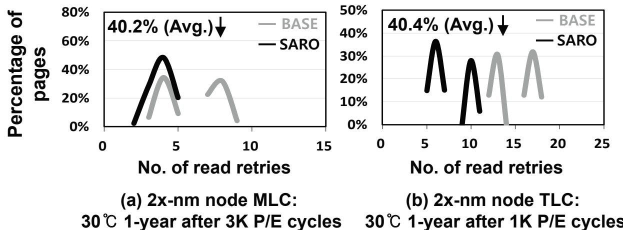

Figure 12: Changes in the number of read retry operations under SARO **over the baseline technique.**

when uncorrectable errors are detected, and repeated until errors can be corrected by the ECC scheme. Since the read latency of a flash device is directly proportional to the number of repeated read retry operations, the read latency is significantly improved when the number of read retry operations is reduced. Figure 12 shows the number of read retry operations under BASE and SARO in MLC and TLC flash chips. SARO reduces the average number of read retry operations by 40% on average over BASE.

6 RELATED WORK

There have been several studies that attempt to improve the reliability of flash devices. Pan *et al.* [7] proposed a technique which can reduce V_{ispp} with P/E cycles to optimize the reliability and performance of NAND flash memory. However, this technique changes V_{ispp} of all program states without considering different error patterns among different program states. Therefore, this technique is rather limited to apply for high-density flash devices, such as TLC flash devices. Park *et al.* [8] also proposed a technique which can change program operating parameters according to P/E cycles. However, their technique is different from SARO in that they did not explore per-state error characteristics. In addition, their technique targets SLC flash devices only so that it cannot be applied for high-density flash devices. The *DPES* technique proposed by Jeong *et al.* [9] is similar to our SARO in that it dynamically changes erase and program parameters of a flash device. However, unlike SARO, it improves the flash endurance only by reducing a stress to flash cells. SARO is different from this technique in that SARO improves the flash reliability in a comprehensive fashion by considering all the different error types including the endurance errors.

7 CONCLUSIONS

We have presented a new flash reliability optimization technique, SARO, that solves the reliability problem of high-density NAND flash memory without sacrificing the program latency. Our proposed technique is based on the state-aware selective programming scheme, which enables each program state to be programmed by a different V_{ispp} value. Since SARO improves the error tolerance of a flash device by selectively reducing V_{ispp} for the most error-prone NAND states only, it is an effective solution to maximize the reliability improvement while minimizing the performance degradation. In order to keep the performance unchanged, SARO parameters are fine-tunned exploiting the flash characteristics that the program latency decreases with cell aging. Our evaluation results with real flash chips show that SARO is effective in improving the flash reliability thanks to the significant decrease in NAND bit errors. It also improves the read latency by 40% on average due to the reduction of read retry operations.

The current version of SARO can be extended in several directions. For example, since a finer V_{ispp} value is more effective for higher flash reliability, we plan to better exploit various system hints (e.g., latency-insensitive program operations) to more aggressively reduce V_{ispp} without affecting the program latency.

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